

FIG. 1

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4		DESTINATION ADDRESS	VADDRESS
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9			
•••	-	PAYLOAD	JAD
max 1639			

FIG. 2

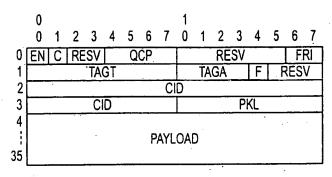
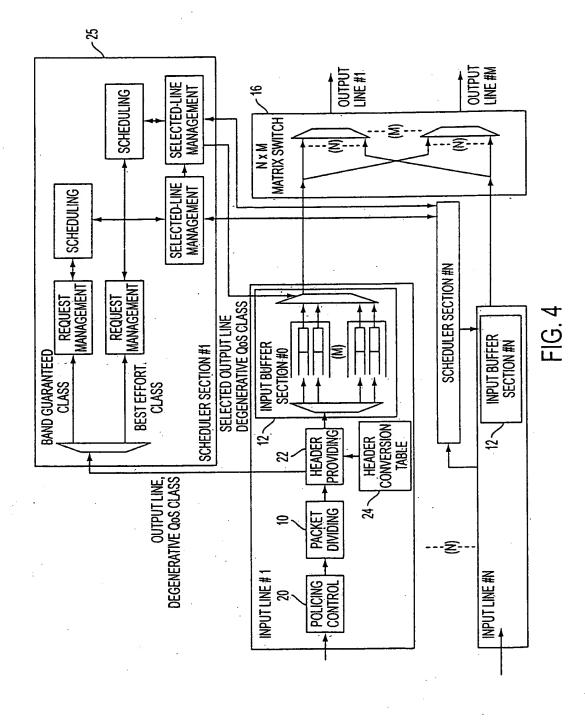


FIG. 3



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										교		교	园	딦	댎	匠	떭	

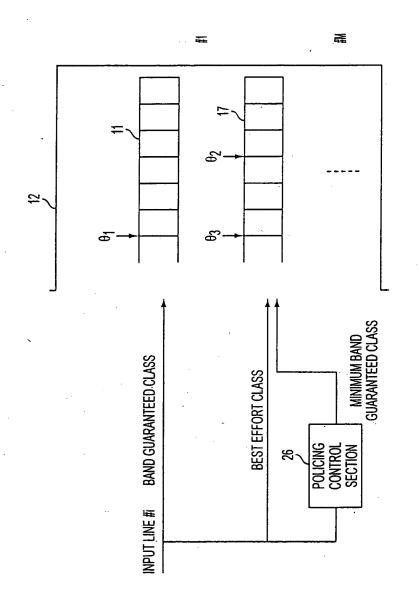
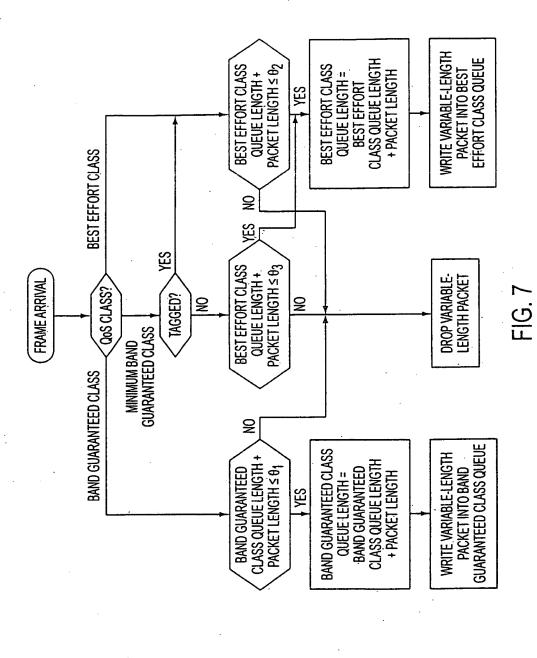


FIG. 6



M.

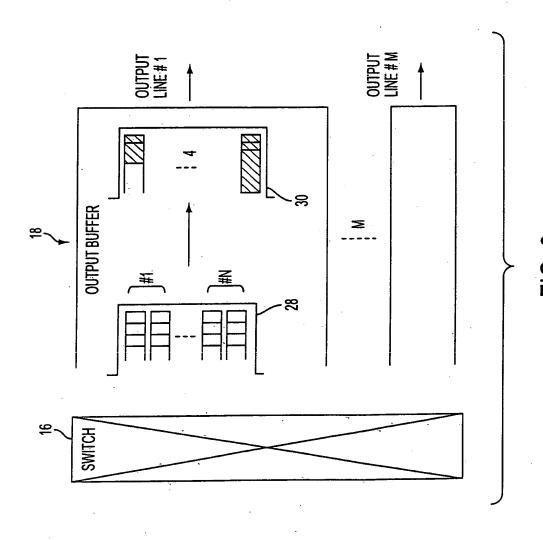
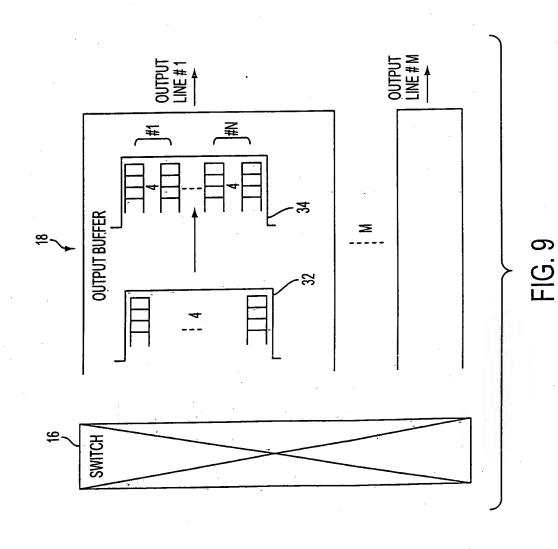


FIG. 8



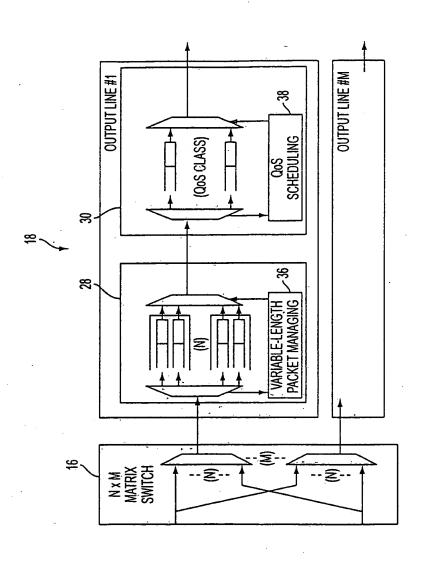
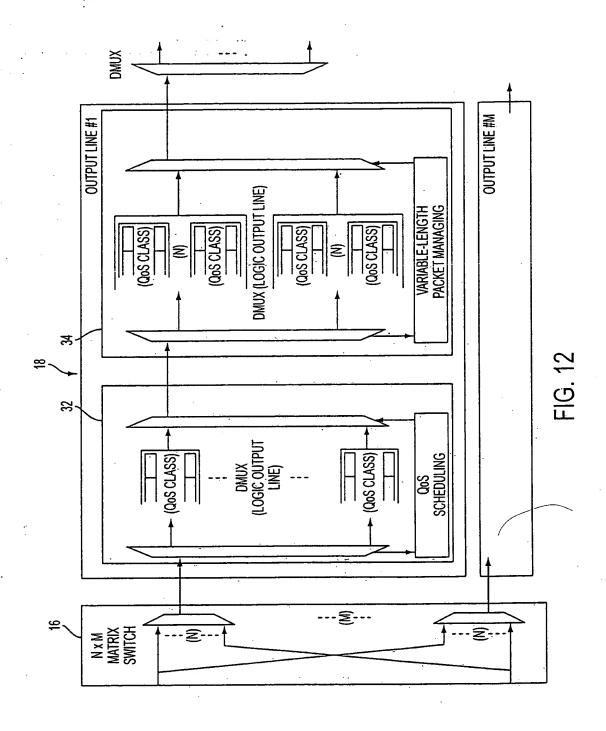


FIG. 11



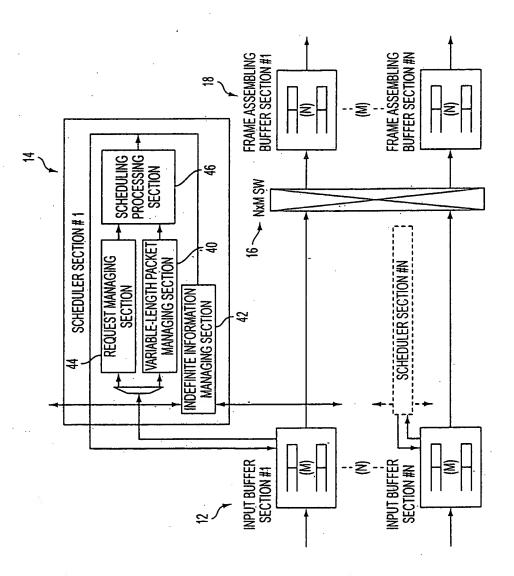


FIG. 13

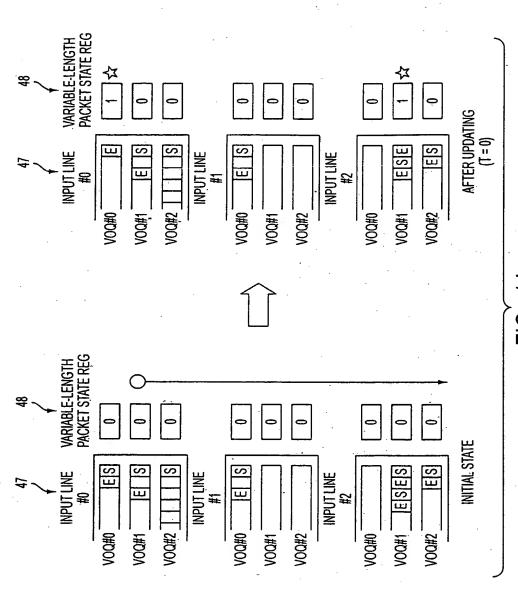


FIG. 14

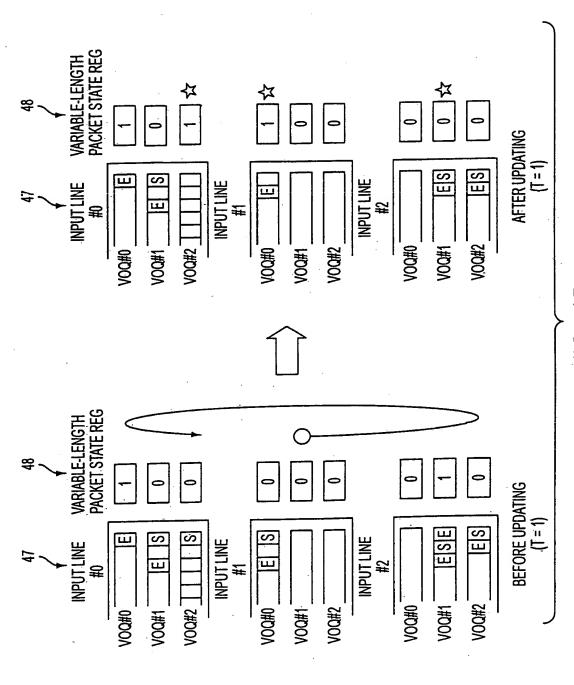


FIG. 15

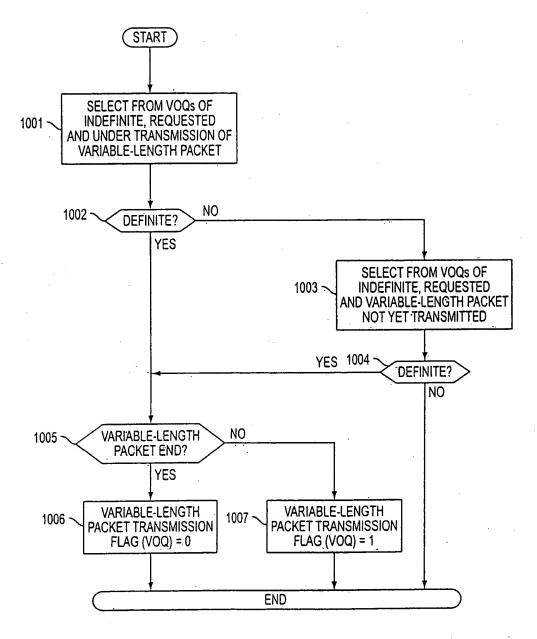


FIG. 16

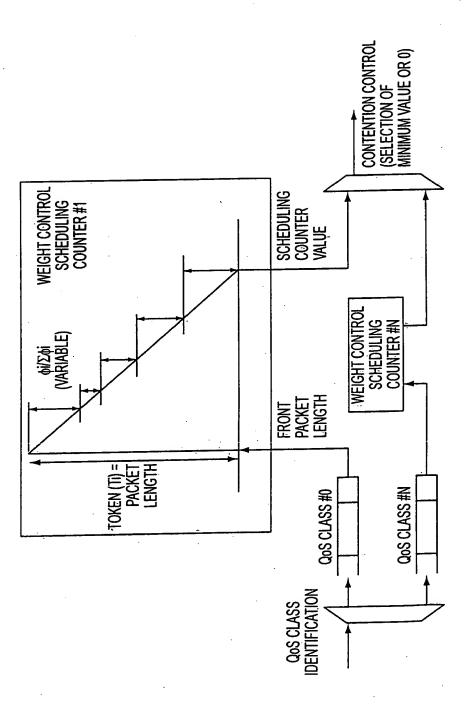


FIG. 17

TO.

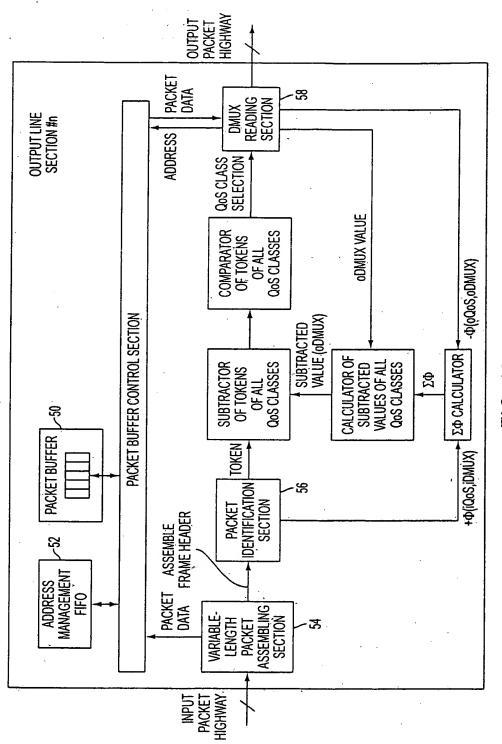


FIG. 18

SU

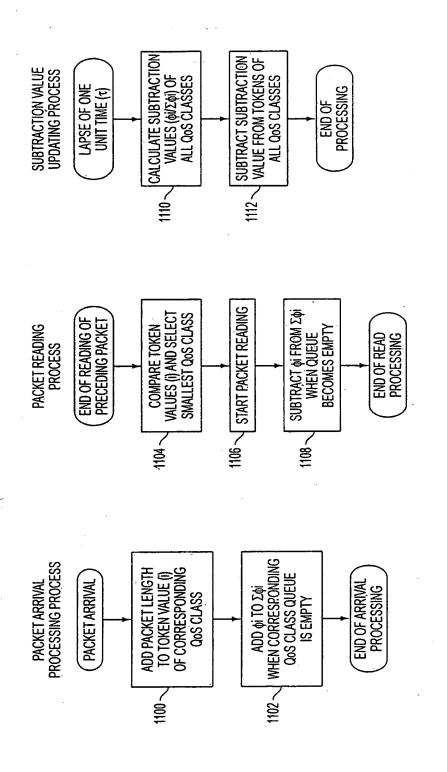


FIG. 19

TO.

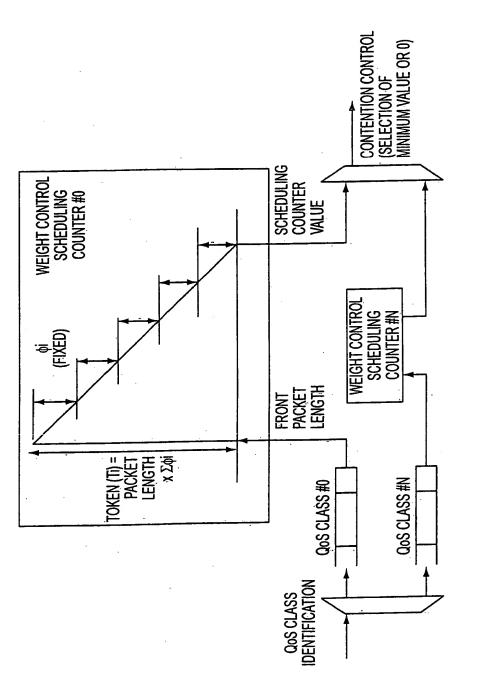


FIG. 20

15.

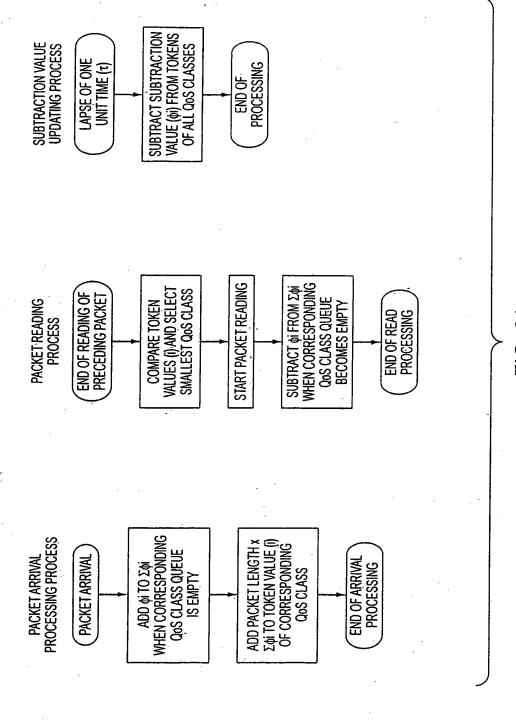


FIG. 21

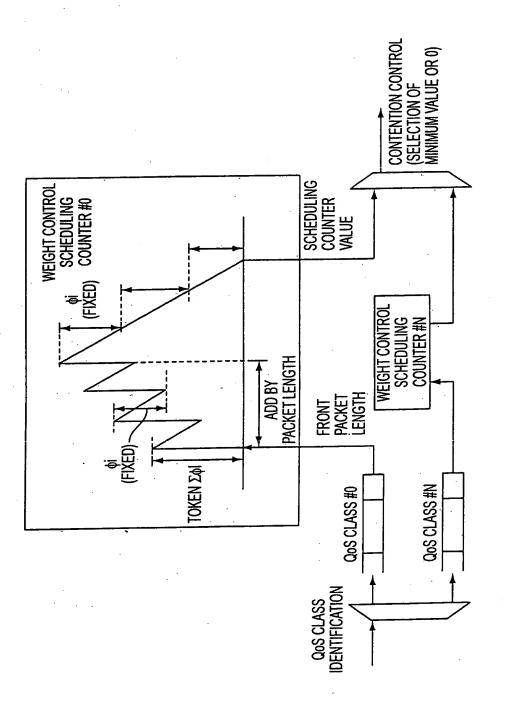


FIG. 2:

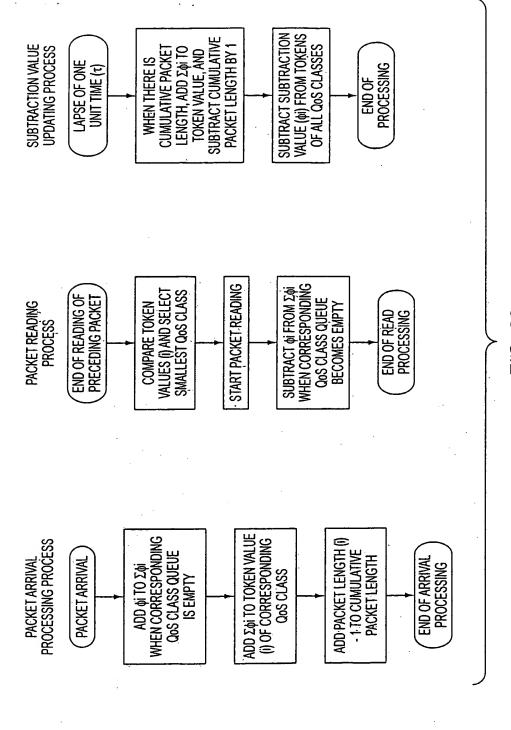


FIG. 23

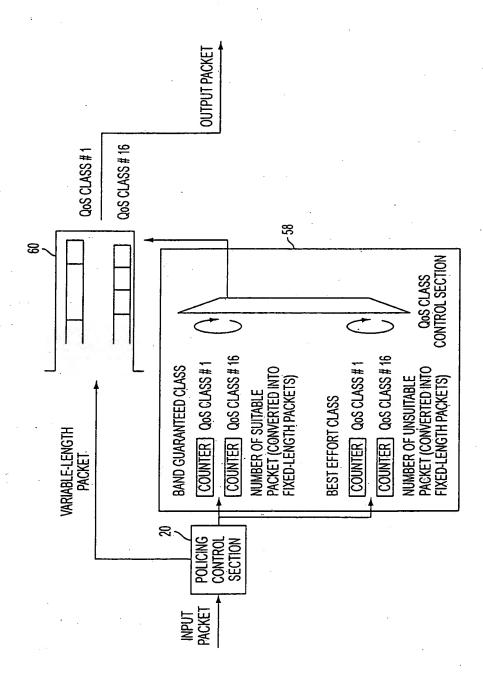


FIG. 24

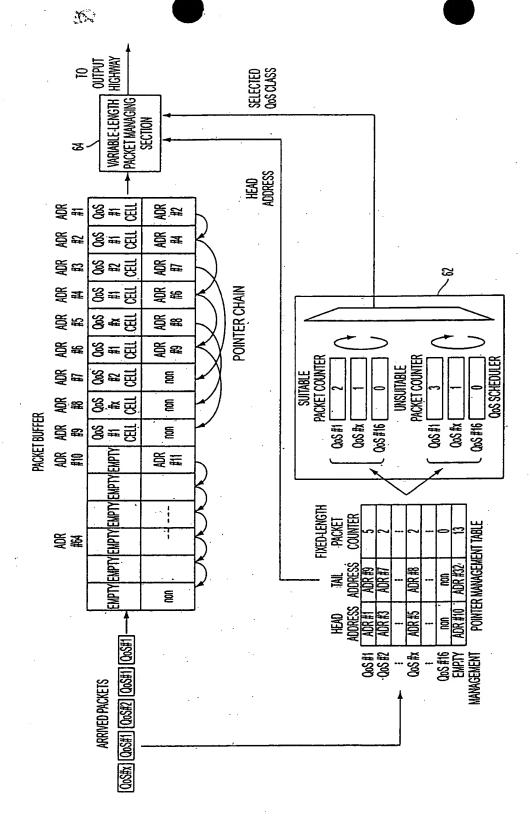


FIG. 25

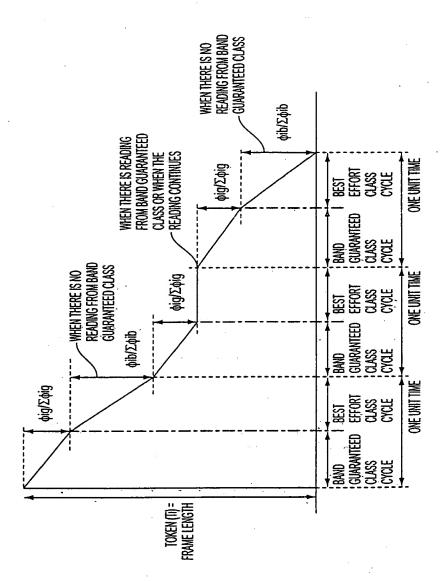
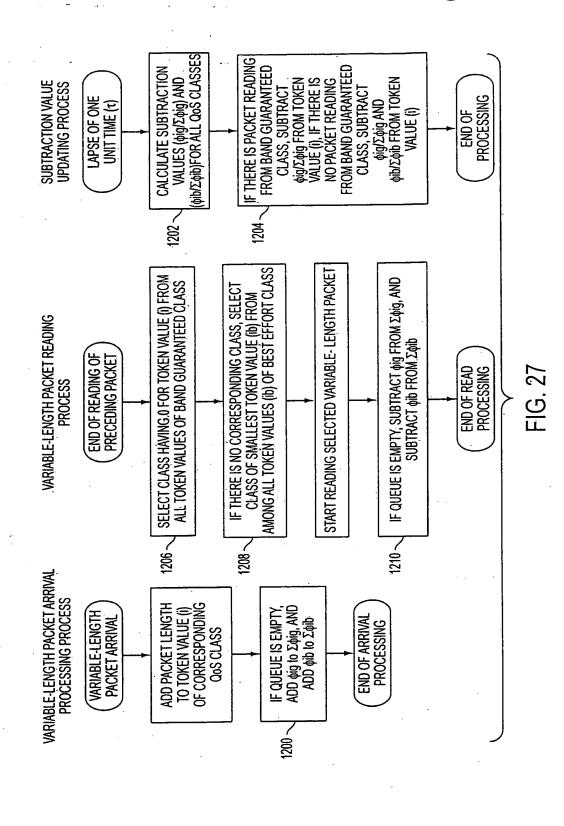


FIG. 26



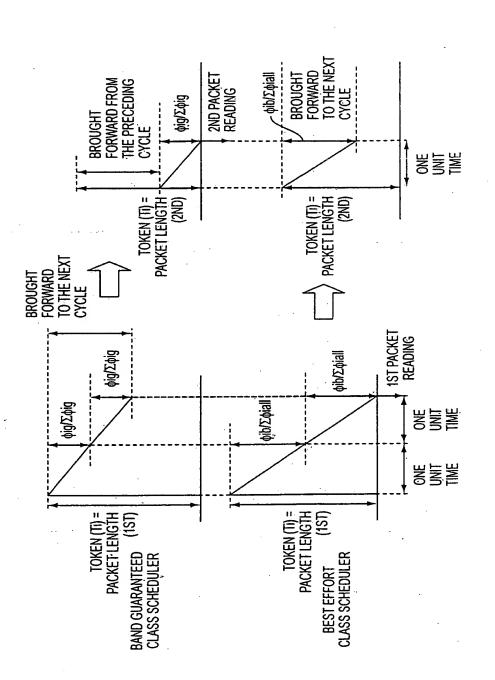
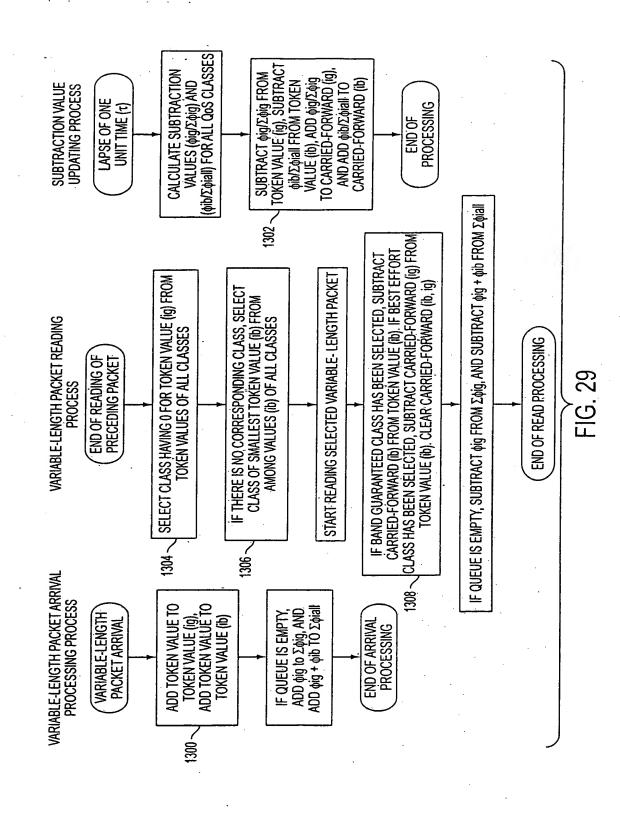


FIG. 28



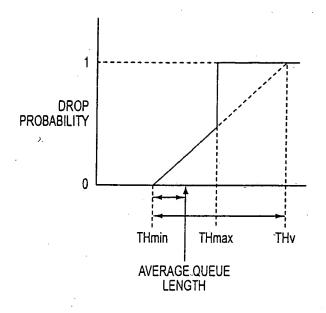
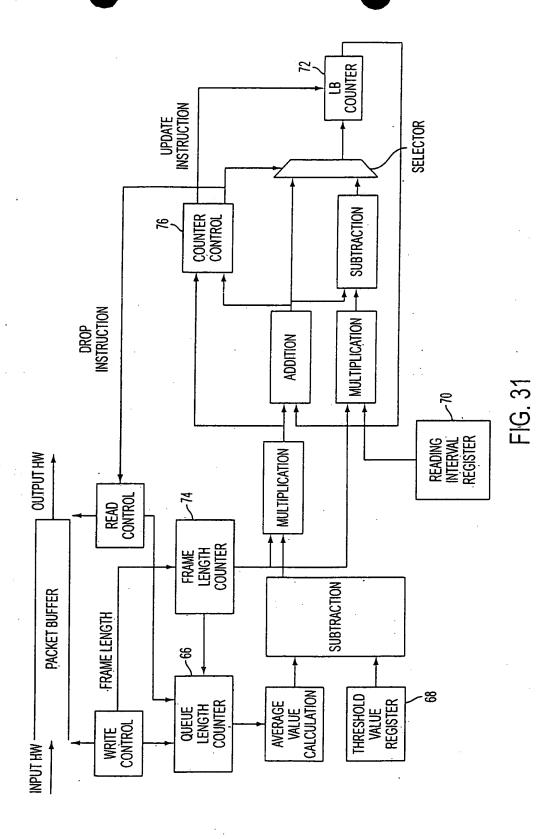
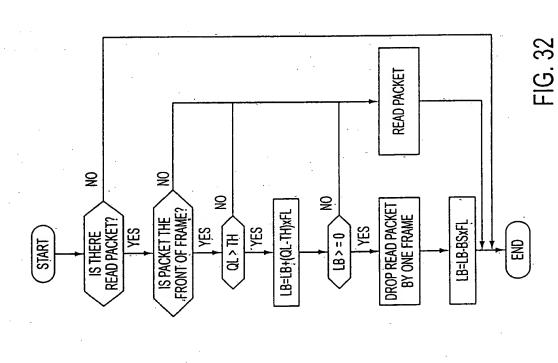


FIG. 30





LB: LB COUNTER QL: (AVERAGE) QUEUE LENGTH TH: DROP THRESHOLD VALUE FL: FRAME LENGTH BS: READING INTERVAL

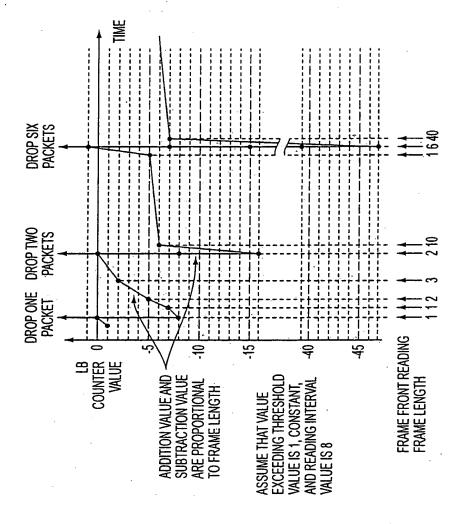


FIG. 33

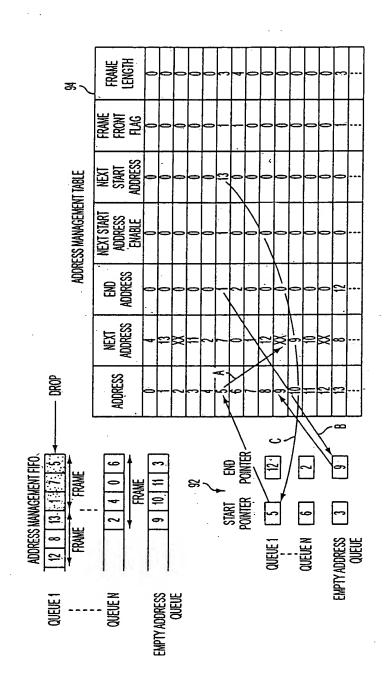


FIG. 34

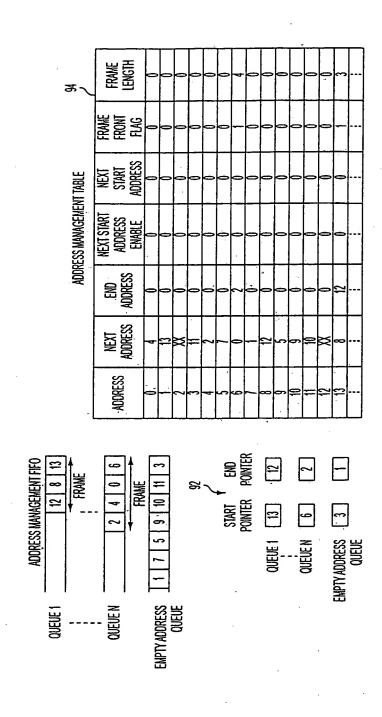
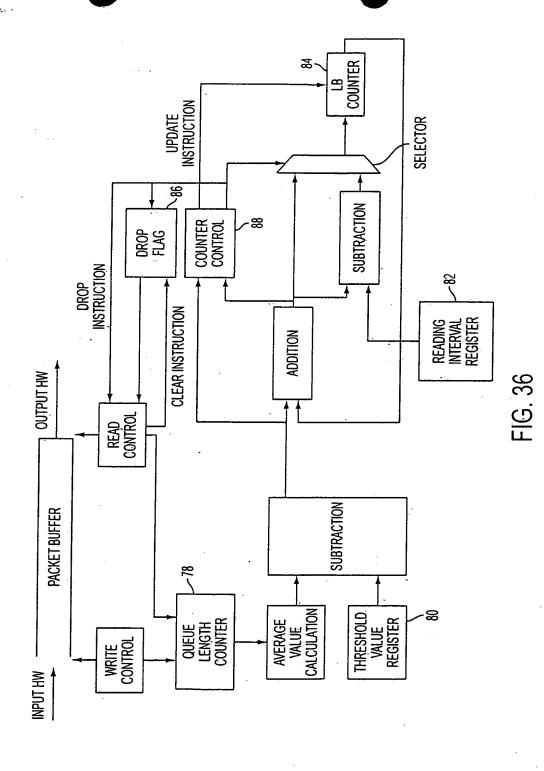
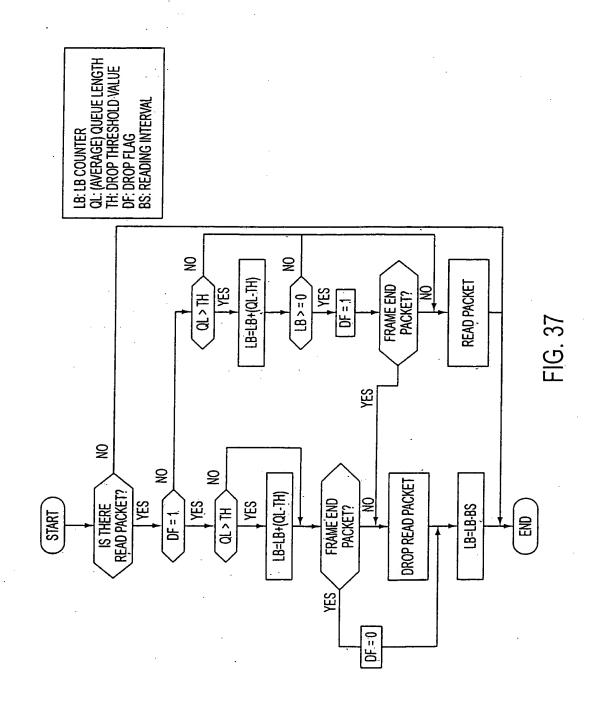


FIG. 33





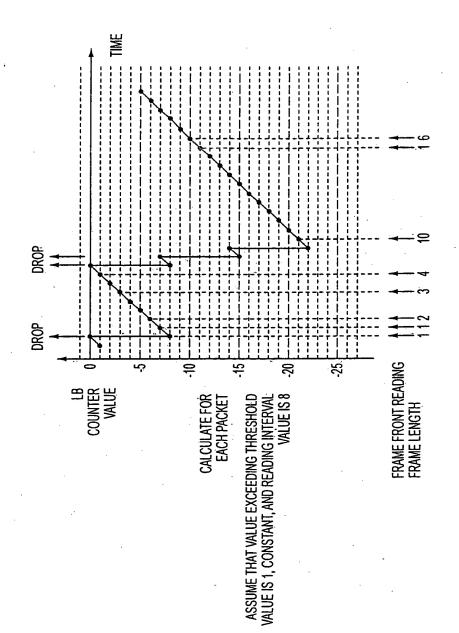


FIG. 38

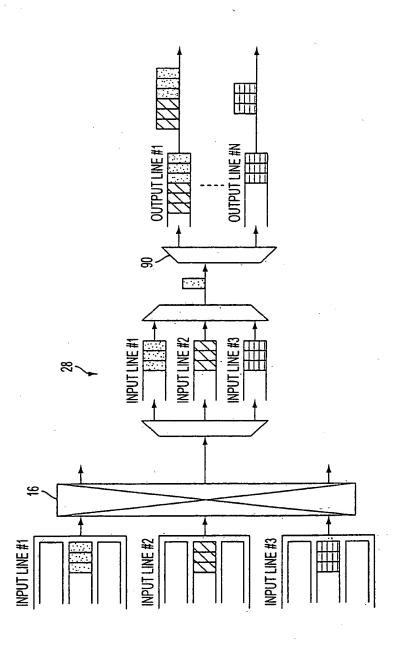


FIG. 39

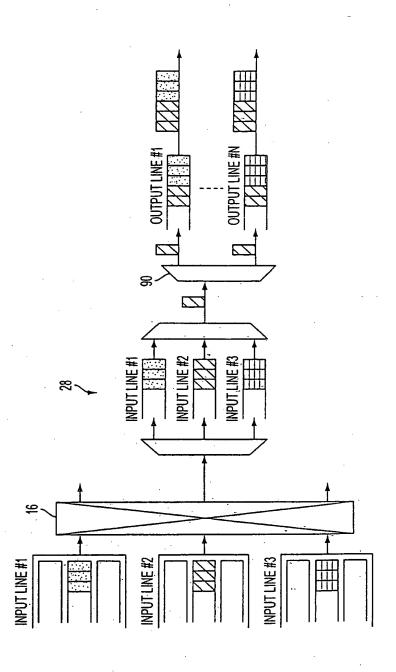


FIG. 4(

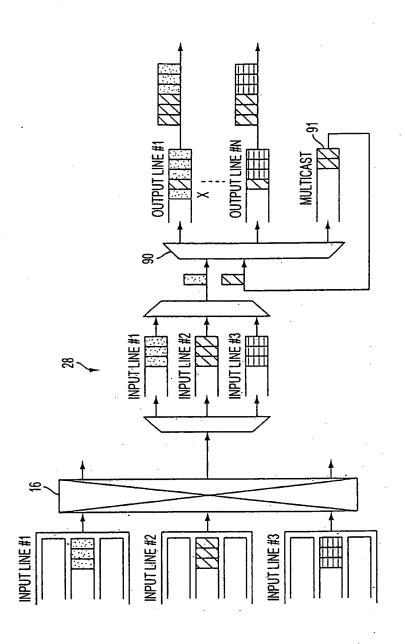


FIG. 4.

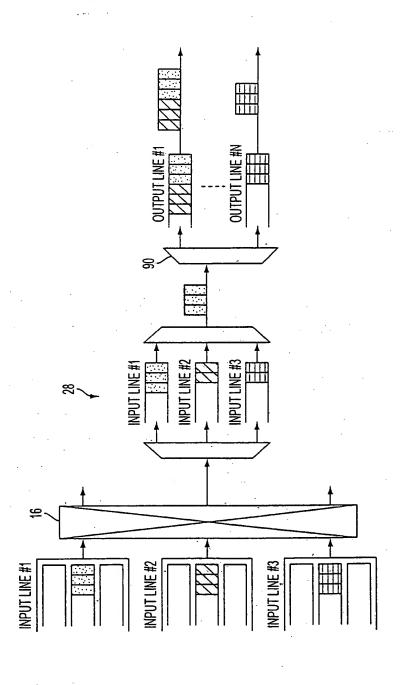


FIG. 4.

....

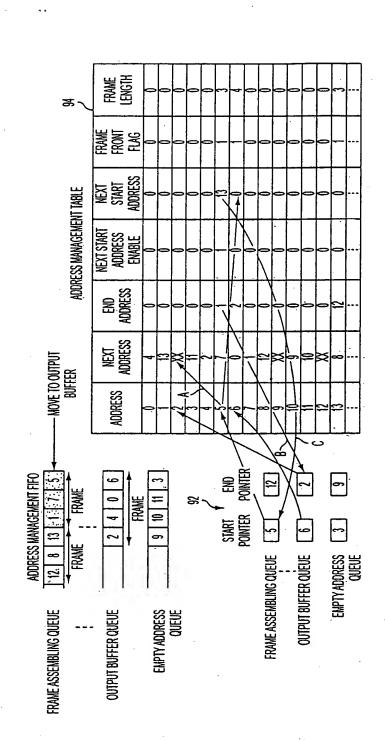


FIG 4

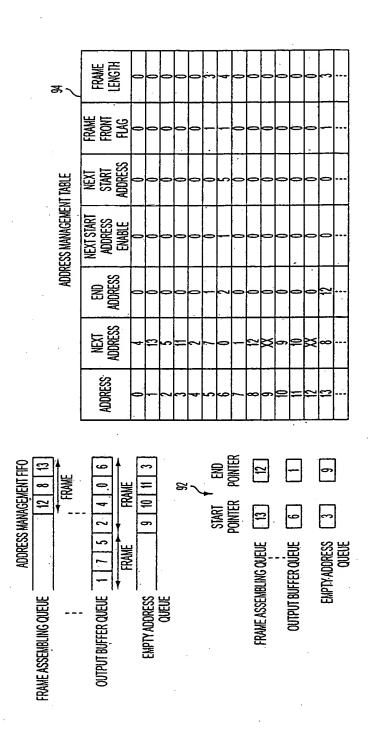


FIG. 42

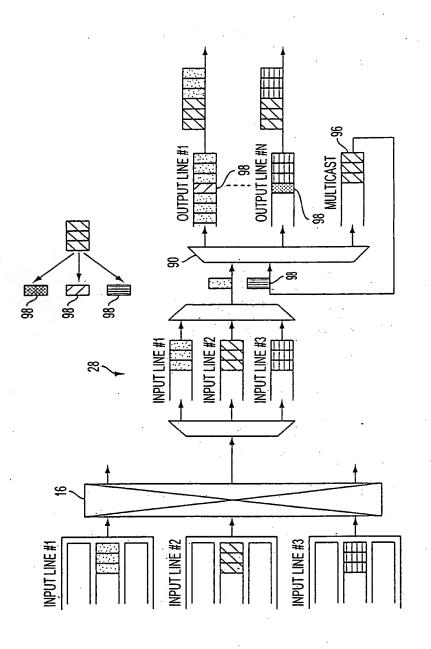


FIG. 45

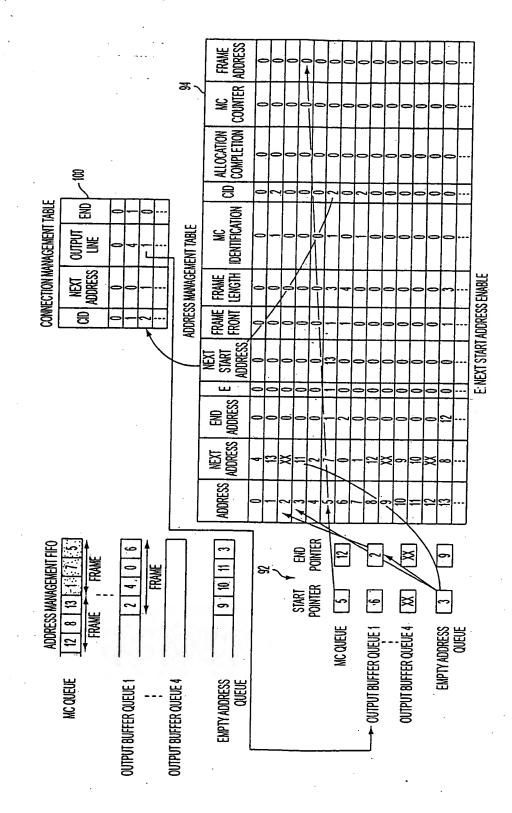


FIG. 46

· .	FRAME ADDRESS		0	~	0	0	0	0	0						
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	END ADDRESS	-		0	3	_	7		> <	0	0	0	2	-	
		4 83	~	= <	7	-	-	- 5	≱ 🌣	6	9	×			
	ADDRESS	1	Ž	7	.	0	3		0	, e	=	2	2		
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PRESS MANAGE 8 13 1 1 RAME 3 2 4 MC FR	6		TOTTO	SIAK STATES]		٥	<u> </u>	≯	[
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MC QUEUE OUTPUT BUFFER QUEUE 1	EMPTY ADDRESS Queue							ייייייי אייייייייייייייייייייייייייייי	OUTFUL BUFFER GUEUE		יטורטו מערובא עטבטב	1012			

FIG. 47

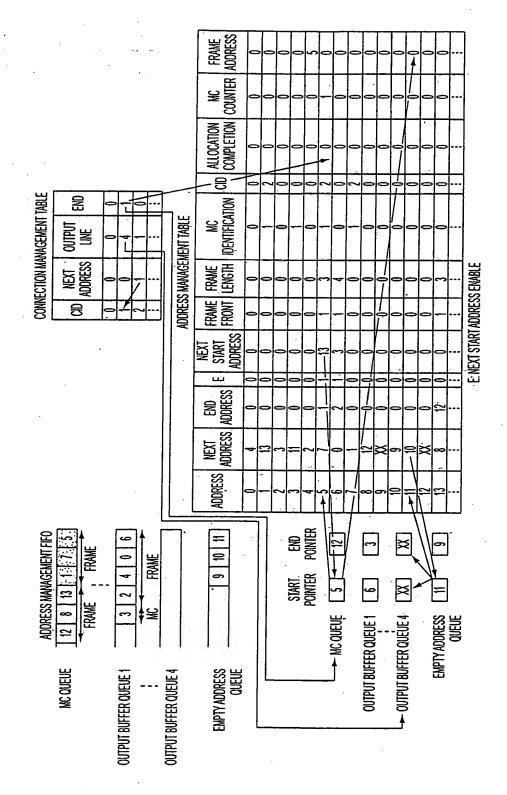


FIG. 48

CID NEXT OUTPUT END 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	MC FRAME IDENTIFICATION CIDENTIFICATION COUNTER ADDRESS 0 0 0 0 0 0	
CID NEXT OUTPUT O 0 0 1 0 4 2 1 1 S 1 1 ADDRESS MANAGEMENT TABLE	ADDRESS ADDRESS E START FRAME FRAME OF 0 0 0 0 0 0	1 13 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
MC QUEUE MC QUEUE MC QUEUE 12 8 13 FRAME OUTPUT BUFFER QUEUE 1 MC FRAME 11		START END POINTER POINTER MC QUEUE [13] [12] OUTPUT BUFFER QUEUE 4 [1] [1] EMPTY ADDRESS [10] [9]

FIG. 49

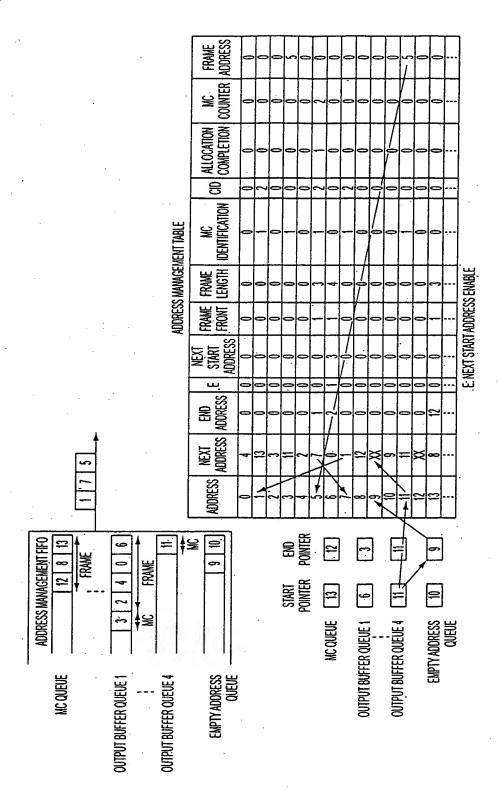


FIG. 50

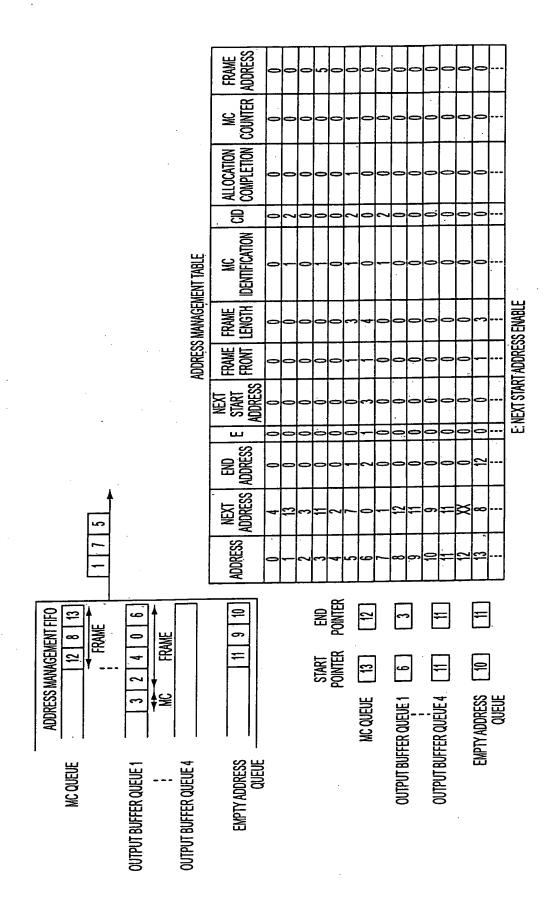


FIG. 51

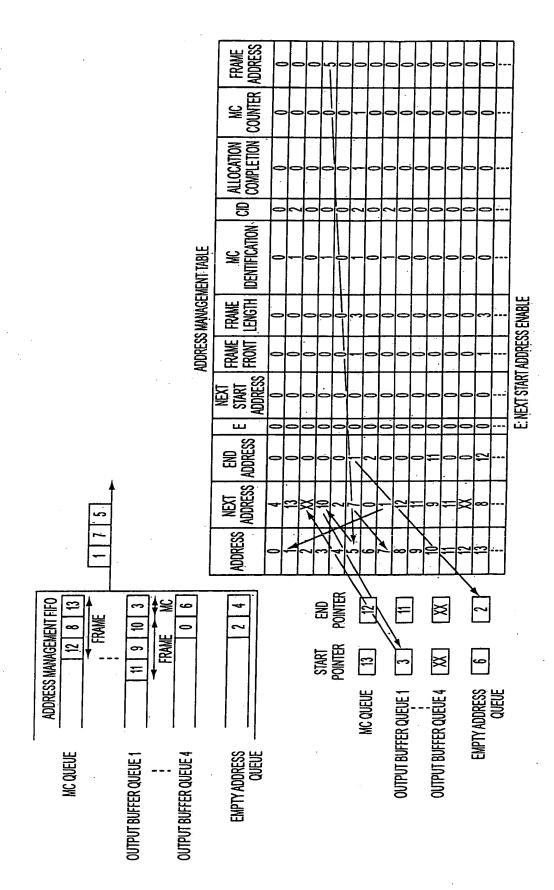


FIG. 52

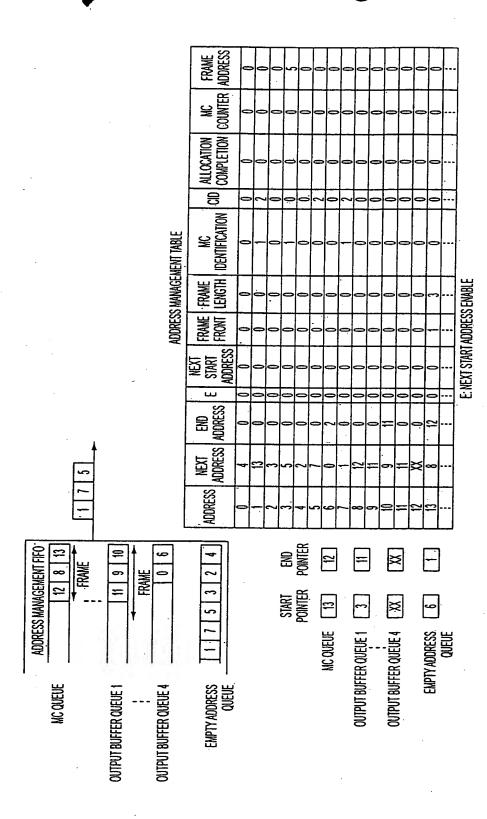


FIG. 53

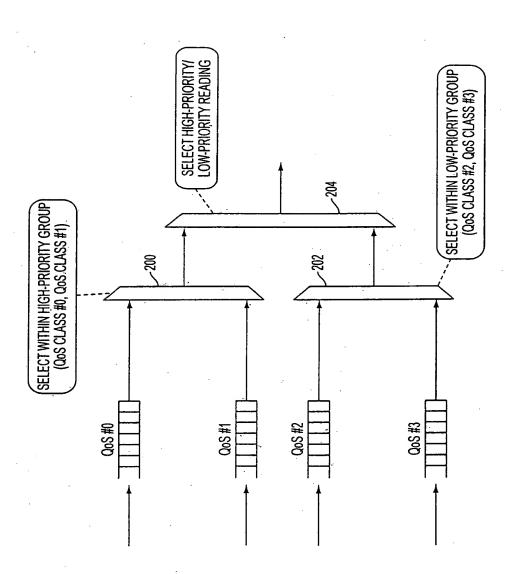
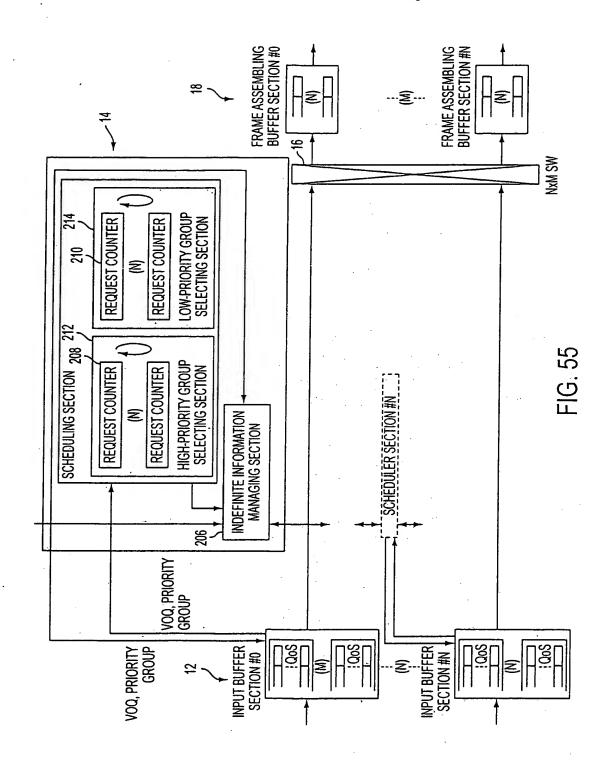
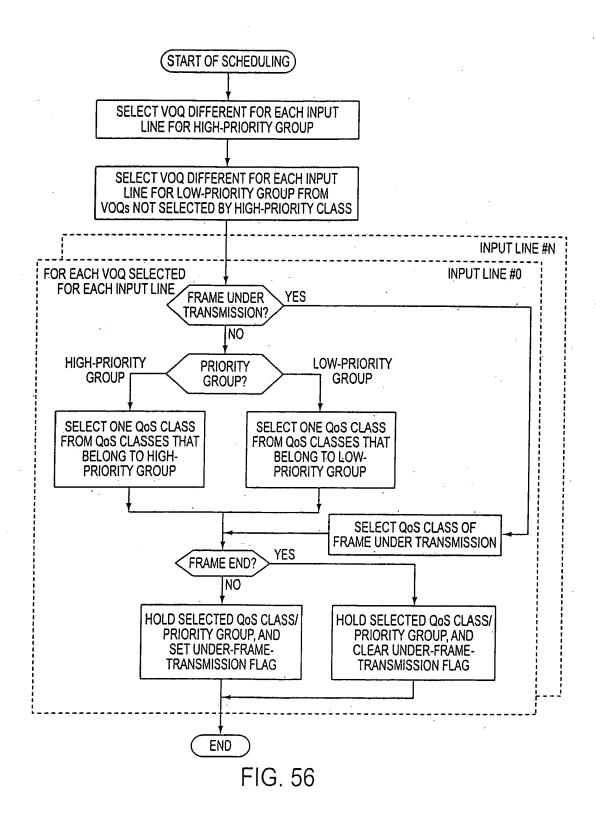


FIG. 54





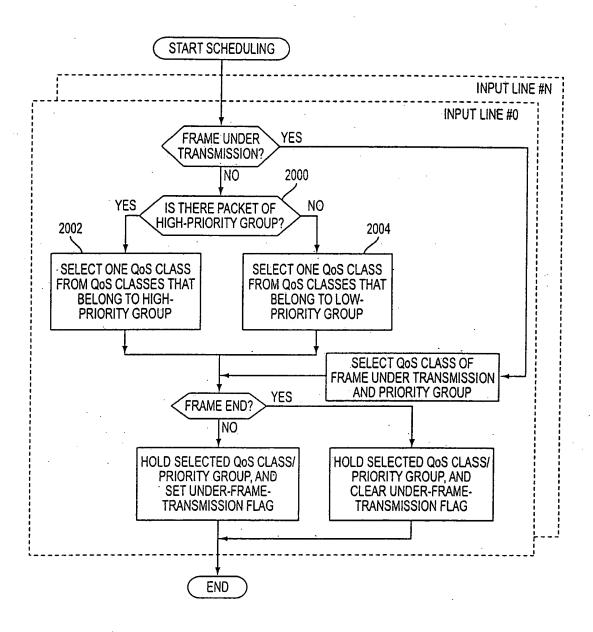
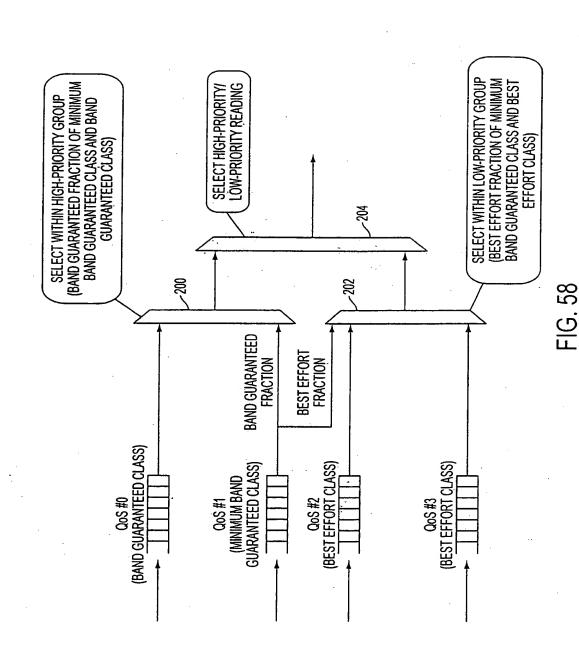


FIG. 57



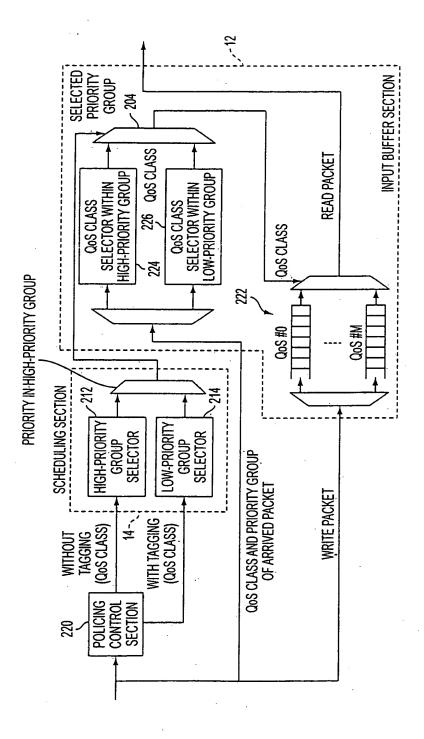
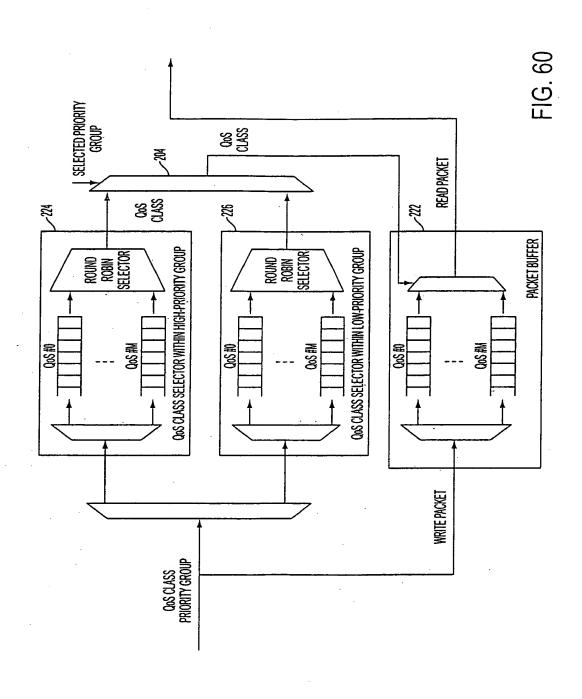
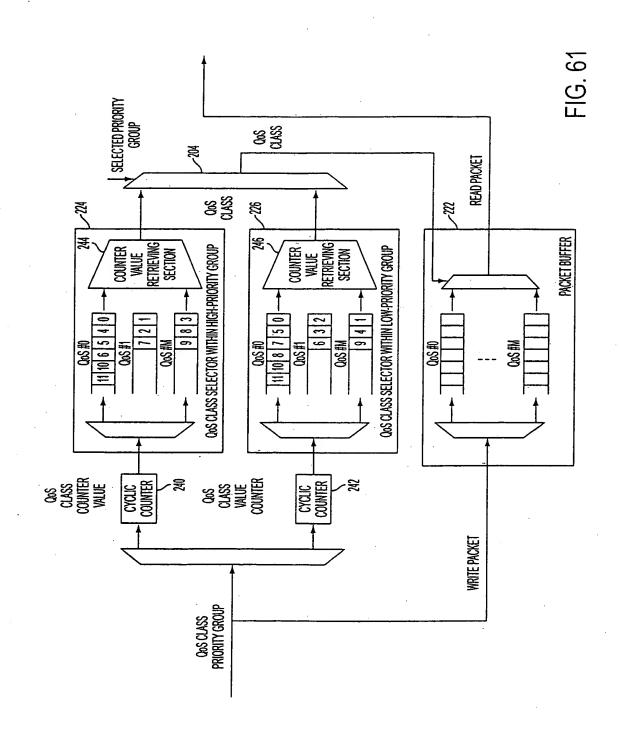


FIG. 59





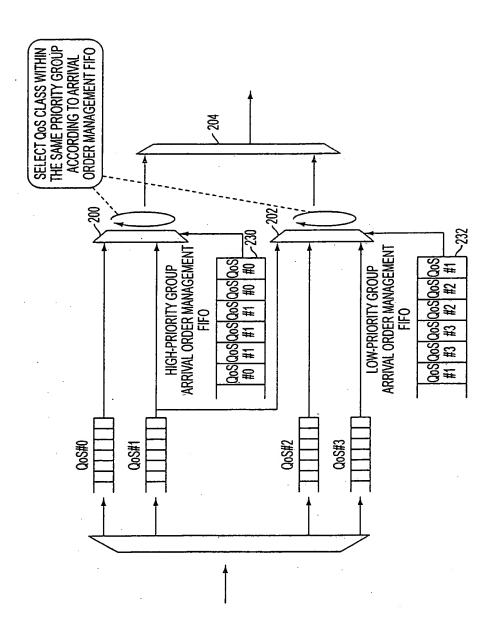


FIG. 62

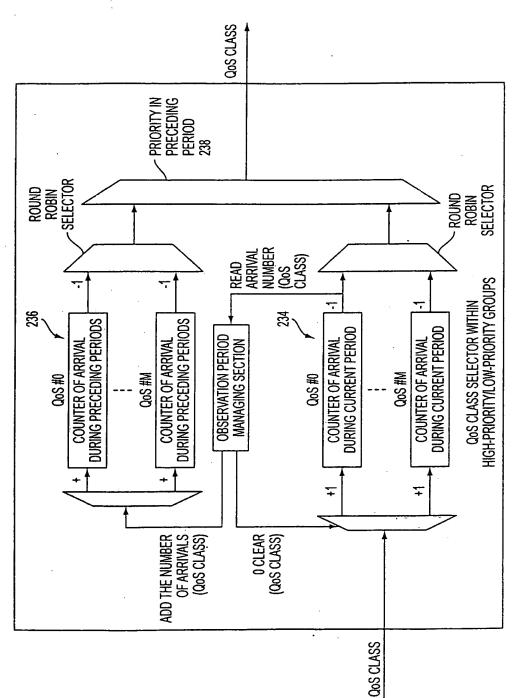


FIG. 63

